Above: MIT has taped out its op amp alternative on IBM's 90nm cmos process.

Obviating op amps

Overcoming the limitations of op amps in high gain, high speed feedback loops. By **Paul Dempsey**.

Like many aspects of analogue design, operational amplifiers (op amps) encounter numerous obstacles when scaled in cmos: specifically, signal swing and intrinsic device gain are reduced. Decreases in gain are a particular problem because, for a feedback based analogue signal processing system, this value determines output accuracy.

Massachusetts Institute of Technology (MIT) unveiled its first step towards obviating the need for op amps in sampled data systems at the 2006 International Solid State Circuits Conference (ISSCC) and disclosed more progress at the same event in San Francisco this February. In the next few weeks, it hopes to announce a further breakthrough – scaling its prototypes from 180nm to 90nm.

But first, a little history. For Hae-Seung Lee, a professor in MIT's Department of Electrical Engineering and Computer Science, the 'Eureka' moment came during a presentation at an earlier ISSCC.

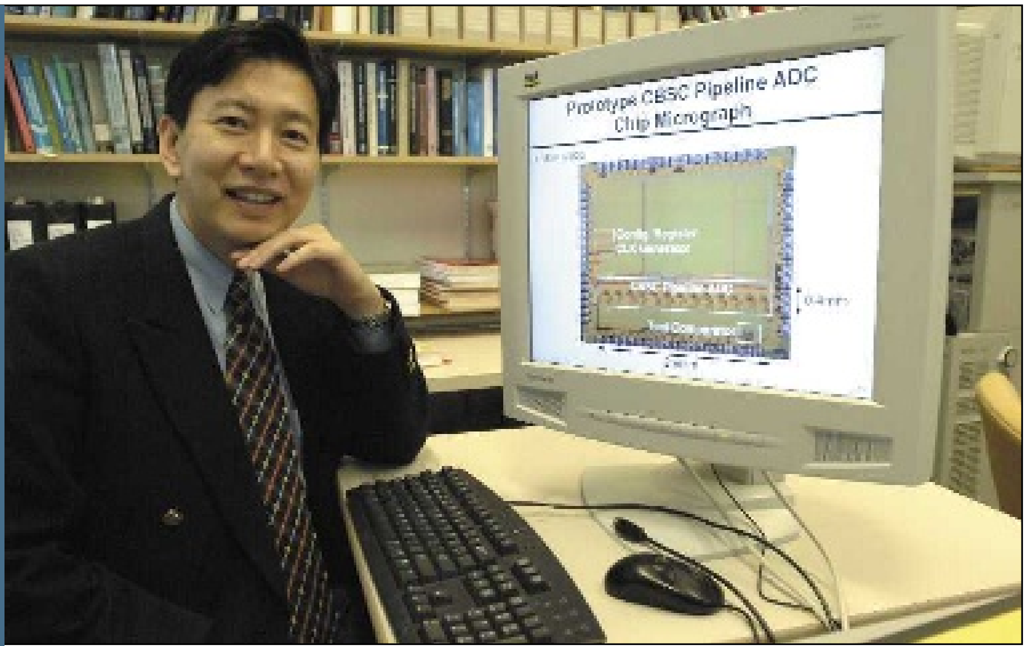
"I'd been working for several years on how various analogue circuits would survive as cmos processes continued to scale, and op amps were obviously becoming more of a bottleneck," said Prof Lee.

"I was at an ISSCC session on cmos imaging and there was a paper that described using a comparator to reset a pixel. That triggered me to think that comparators could do things other than what they had originally been designed for. On the way back from the conference, I began thinking that maybe we could replace op amps with comparators."

The resulting comparator based switched capacitor circuit (CBSC) was described in prototype form 18 months ago *[1]*. It was fabricated on an 180nm National Semiconductor process and was the result of a broad collaboration between Prof Lee's team, that of his MIT colleague Professor Charles Sodini and NatSemi.

A key innovation was that where, traditionally, a high gain op amp was needed to force the virtual ground mode at the input to the conversion process, by swapping in the comparator, the device could simply detect it. Some dc bias current was consumed in both cases, but this was significantly lower for the comparator based design – a vital requirement for many end applications and especially those in consumer electronics.

"So, we essentially achieved the same functionality in prototype form as you got from an op amp, but with detection done by a comparator. The next stage was to see how we could take the effi-



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Prof Hae-Seung Lee, **MIT**

ciencies further," Prof Lee continued.

A comparator typically takes two arbitrary voltages and determines which is larger. To perform that function, most comparators have amplifiers followed by a latch. The amplifiers take a dc bias current and burn some power. Having put comparators into a more power efficient form for an a/d converter than an op amp, the MIT researchers then recognised that the input voltages to the comparators in the CBSC circuit were not really arbitrary. Rather, they were very well defined: even waveforms using a ramp, and always approaching from the same direction.

"Because the voltages were so deterministic, that meant that we could replace the comparator, this time with a zero crossing detector that could be built using a simple precharged logic circuit, rather than amplifiers. Once we had the precharged logic circuit – which we call a dynamic zero crossing detector (DZCD) *[2]* – we could pretty much eliminate the dc bias element, so the overall power consumption is lower still," Prof Lee claimed.

If implemented in commercial silicon, the DZCD will require extra features. Whilst its threshold is a function of ramp rate, process and temperature, no auto zeroing mechanism was implemented in the prototype to overcome these dependencies, although Prof Lee believes this will be straightforward.

Persistent issues

However, a more persistent issue is that the single ended nature of the circuit currently makes it unsuitable for high resolution circuits.

The same problem is dogging many other attempts to realise traditionally analogue circuitry in a digital form, although Prof Lee is confident that raising the DZCD from its current 8bit resolution and 200Msample/s capability to 12bit, albeit at 100Msample/s, might be achieved within the next two years.

Prof Lee suggests that, because the DZCD is more open to implementation in differentiated topologies, 16bit is theoretically possible. This flexibility means the technology may not be as vulnerable to power supply and substrate noise as other proposed analogue to digital design switches, particularly when integrated as part of a system on chip.

In the nearer term, however, one objective has been more firmly secured. Following on from the CBSC, the DZCD was originally prototyped in 180nm cmos with an active die area of 0.05mm≈ and fabricated at TSMC.

"Obviously, scaling is a big driver for the technology, but we have so far been limited by the technologies that we, as a university, could get access to and those were the processes that were available at the time," says Lee. "However, we now have access to IBM's 90nm cmos process. Obviously, we'd really like to get access to 65nm, but we have taped out at 90nm and – although we don't yet have silicon – we do know that the technology scales."

So will MIT's op amp alternative make it to market? Although senior engineers at both National Semiconductor and Analog Devices have picked the technology as 'one to watch', Prof Lee is being conservative.

"We have had commercial interest," he says, "But, from their [the semiconductor companies'] point of view, there are still quite a few risk factors. Although I don't see any showstoppers, that doesn't mean there isn't a hidden showstopper somewhere. In terms of putting the technology directly into a product, I would say we're talking about a few years."

In a Rumsfeld-esque summation, Prof Lee noted: "The real challenge is that we don't know what the real challenges are yet. And we won't until we do more research and try to push performance, speed and accuracy."

The work of Prof Lee and his colleagues answers a direct and growing design roadblock. MIT's papers on replacing the op amp have consistently attracted attention and further news will be eagerly anticipated.

References

[1] Comparator based switched capacitor circuits for scaled cmos technologies. Todd Sepke, John K Fiorenza, Charles G Sodini, Peter Holloway, Hae-Seung Lee. Proc. ISSCC 2006, pp 220-21 & 649

[2] A zero crossing based 8b 200MS/s pipelined ADC. Lane Brooks, Hae-Seung Lee. Proc. ISSCC 2007, pp 460-61 & 615.